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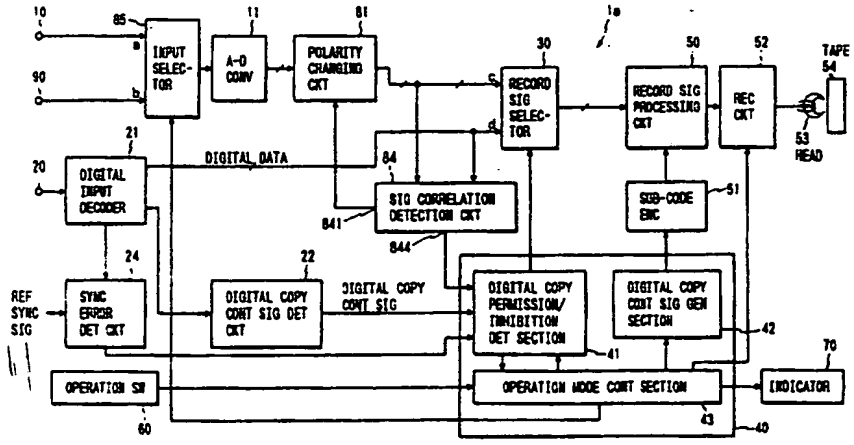
(54) Data recording apparatus.

(57) A data recording apparatus comprises a digital input processing circuit, an analog input processing circuit including an A/D converter for recording the analog input signal in a digital form, a switch for selecting either digital or analog input signal for recording, and a control circuit. Normally, the apparatus records the digital input signal. When the digital input processing circuit detects a synchronizing error or inhibition of recording the digital input signal (digital copy) by analyzing the sub-code signal of the digital input signal, the control circuit control the switch so as to select the analog input signal. In order to reduce unnatural level variation due to change of selection between the digital and analog input signals, there are further provided a polarity change circuit, variable delay, and variable gain amplifier for the analog audio signal.

FIG. 1



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DATA RECORDING APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a data recording apparatus.

2. Description of the Prior Art

A data recording apparatus capable of selectively recording digital and analog audio signals is known. A product of Matsushita electric industry corp. (model number; SV-D1000) have been sold since 1987 as a digital • audio • tape recorder (hereinbelow also referred to as DAT). Fig. 10 is a block diagram of this DAT. In Fig. 10, numeral 11 is an A/D converter. Numeral 21 is a digital input decoder for decoding a digital input signal, from a terminal 20, specified by a standard (IEC-958) of a digital audio interface to produce digital audio and sub-code signals. Numeral 22 is a digital copy control signal detection circuit for detecting a digital copy control signal included in the sub-code signal. Numeral 24 is a synchronizing error detection circuit for detecting errors in bit synchronizing or frame synchronizing. Numeral 30 is a record signal selector for selecting either output signal of the A/D converter 11 or an output signal of the digital input decoder 21. Numeral 31 is a muting processing circuit for muting the record signal. Numeral 400 is a system controlling section for controlling operation of the system. The system controlling section 400 comprises a microprocessor for controlling the whole system through communication through its input and output ports with peripheral circuits and logical calculation processing therein. As structure of the microprocessor (mpu) is well-known, thus, the detailed description is omitted. Fig. 11 shows a flow chart showing flows of controlling operation of the prior art DAT shown in Fig. 10. A program stored in the system controlling section 400 is provided such that the system controlling section 400 operates in accordance with the flow chart of Fig. 11. Numeral 410 included in the system controlling section 400 is a permission/inhibition determination section for making determination as to permission/inhibition of digital copying in accordance with the digital copy controlling and synchronizing error detection signals. Numeral 420 is a digital copying recording controlling signal generation section included in the system controlling section for generating a digital controlling signal to be recorded on the recording medium. Numeral 51 is a sub-code encoder for converting the digital copy controlling signal into a sub-code formatted signal. Numeral 50 is a record signal processing circuit for converting the audio digital and sub-code signals into a record format signal. Numeral 52 is a recording circuit. Numeral 53 is a head. Numeral 54 is a magnetic tape. Numeral 60 is a operation switch. Numeral 70 is an indicator.

Operation of the prior art data recording apparatus having the above-mentioned structure will be described with reference to Fig. 11 showing operation. Fig. 11 shows a flow chart of controlling operation of the system controlling section 400. When a command for digital copy mode is made by the operation switch 60 (step 202), an operation mode controlling section 430 included in the system controlling section 400 controls the record signal selector 30 to select the digital input signal from the terminal 20. At the same time, the mpu detects synchronizing condition and determines permission/inhibition digital copying. If the result shows "permission", it causes the recording circuit 52 to be in recording condition (step 205) from the digital copy control signal. If the result shows "inhibition", it prevents the recording circuit 52 to be in the recording condition and indicates "digital copying is forbidden" and provides flickering indication to promote some counter operation (step 206).

Hereinbelow will be described condition detection after it enters a digital copy recording mode (step 205) and operation thereof. After start of recording (step 205) with selection of the digital input signal, mpu detects synchronizing error and digital copy controlling signal (steps 207 and 209). If synchronizing is not in error and the digital copy controlling signal indicates permission of copying, the mpu maintains the digital copy operation (step 211). If synchronizing is in error and the digital copy controlling signal indicates inhibition of copying, it controls the muting processing circuit 31 so that a muted signal is recorded (step 211).

An error in synchronizing may occur because the receiving side cannot respond the change of the sampling frequency when a sampling frequency of the digital signal is changed. For example, when a satellite broadcasting signal is received directly, a synchronizing error occurs when the mode is changed between A and B. This is because sampling frequencies of A and B modes are different each other. Then, for the synchronizing error interval, the muted signal is recorded. Further, if the number of generations of copy permitted is

specified and is recorded on a recording medium for protecting copyright, and when this magnetic tape is reproduced, the digital copying controlling signal may change from permission to inhibition of digital copying. Thus, if copying is carried out from such a magnetic tape to other magnetic tape, some portion of another magnetic tape includes muted portions so that the copied tape becomes different one from one that the operator intended to make. In other words, the recorded program is not in continuous.

According to the above-mentioned prior art, the operator can carry out digital copying if the operator acknowledges that the input signal is one permitted for digital copying. However, if the operator does not know such information, once the operator tries to set digital copy mode and record so that he is informed of permission or inhibition of digital copying. As mentioned, it is very inconvenient that the operator does not know whether digital copying is permitted or not when he record the digital audio input signal by the DAT because there are digital audio signals for which digital copy is permitted and not permitted. This inconvenience has been reduced as follows:

If an analog signal is available from the same source, which includes the same content as the digital audio signal includes, the analog signal is supplied to the analog signal input terminal 10 and then the apparatus is changed into analog recording mode in response to the operation switch 60. Then the content can be copied using the analog signal in stead of the digital signal. Further, if synchronizing becomes in error during digital copying or a control signal indicative of inhibition of digital copying occurs during digital copying, a muted signal is recorded and an alarm is displayed. In response to this, the operator temporally stops recording and then he changes the apparatus into the analog recording mode with the operation switch 60. so that he can copy the analog signal including the content as the same as the digital audio signal including. However, there are not only inconvenience that the operator should monitor the recording condition continuously to change the signal for recording and to direct the operation mode again to the apparatus. Further though such trouble is removed, another decisive inconvenience cannot be removed, that a portion of content recorded is lacked due to stop of recording and In other words, sound or the program recorded on the magnetic tape includes incontinuous portions.

In order to remove this problem, this invention provides data apparatus for maintaining copy operation even if a condition of digital input signal changes during digital copying.

SUMMARY OF THE INVENTION

The present invention has been developed in order to remove the above-described drawbacks inherent to the conventional data recording apparatus.

A data recording apparatus comprises a digital input processing circuit, an analog input processing circuit including an A/D converter for recording the analog input signal in a digital form, a switch for selecting either digital or analog input signal for recording, and a control circuit. Normally, the apparatus records the digital input signal. When the digital input processing circuit detects a synchronizing error or inhibition of recording the digital input signal (digital copy) by analyzing the subcode signal of the digital input signal, the control circuit control the switch so as to select the analog input signal. In order to reduce variation due to change of selection between the digital and analog input signals, there are further provided a polarity change circuit, variable delay, and variable gain amplifier.

According to the present invention there is provided a first data recording apparatus comprising; an A/D converter for converting an analog input signal; a digital decoder for decoding a digital input signal to obtain digital data and a synchronizing signal; a selector responsive to a control signal for selecting either an output of the A/D converter or the digital data for recording; synchronizing error detector for detecting synchronizing error through comparison between the synchronizing signal and a reference synchronizing signal; and a controller responsive to an output of the synchronizing error detector for producing the control signal to cause the selector to select the output of the A/D converter when synchronizing error is detected.

According to the present invention there is also provided a second data recording apparatus comprising; an A/D converter for converting an analog input signal; a digital decoder for decoding digital input signal to obtain a digital data and a sub-code signal; a selector for selecting either an output of the A/D converter or the digital data in response to a control signal; a detector responsive to the subcode signal for detecting a copy control signal indicative of permission and inhibition of recording with the digital input signal; and a controller responsive to the detected copy control signal for producing the control signal to cause the selecting means to select the output of the A/D converter when the inhibition is detected.

In each of the first and second apparatus, there is an unnatural variation of the output level of the selector due to change of selecting input signals by selector. Thus, a polarity changing circuit can be

provided to the first and second apparatus to consist the polarity of the analog signal with that of the digital input signal. Further, a variable delay circuit may be provided to the first and second apparatus to consist the phase of the analog signal with that of the digital input signal. Further, a variable gain amplifier may be provided to the first and second apparatus to consist the amplitude of the analog signal with that of the digital input signal. Further, a muting circuit may be provided to the first and second apparatus to mute the input signal when synchronizing error and inhibition of copy are detected respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and features of the present invention will become more readily apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

Fig. 1 is a block diagram showing a first embodiment of a data recording apparatus of the invention;

Fig. 2 shows a flow chart showing flows of controlling operation of the data recording apparatus of embodiments throughout the specification;

Fig. 3 shows interconnection between this apparatus and external apparatus, which is suited for embodiments throughout the specification.

Fig. 4 is a block diagram of polarity changing circuit shown in Figs.1, 8, and 9;

Fig. 5A is a block diagram of the signal correlation circuit 84 of embodiments throughout the specification;

Fig. 5B shows a block diagram of the peak detectors shown in Fig. 5A;

Fig. 5C is a block diagram of the time difference detector shown in Fig. 5A;

Fig. 6 is a block diagram showing the second embodiment of the invention;

Fig. 7 is a block diagram showing the third embodiment of the invention of the data recording apparatus;

Fig. 8 is a block diagram showing the fourth embodiment of the invention of the data recording apparatus;

Fig. 9 is a block diagram showing the fifth embodiment of the invention of data recording apparatus;

Fig. 10 is a block diagram of data recording apparatus of a prior art; and

Fig. 11 shows a flow chart used in the prior art of Fig. 10.

The same or corresponding elements or parts are designated at like references throughout the drawings.

DETAILED DESCRIPTION OF THE INVENTION

Hereinbelow will be described a first embodiment of a data recording apparatus of the invention with reference to drawings. Fig. 1 is a block diagram showing a first embodiment of the data recording apparatus of the invention. Fig. 2 shows a flow chart showing flows of controlling operation of the DAT shown in Fig. 1 of the embodiment of the invention. In Fig. 1, an analog audio input signal is applied to "a" input of an auxiliary input selector 85 through a terminal 10. Another analog audio input signal is also applied to "b" input of the input selector 85 through a terminal 90. The auxiliary input selector 85 selects either analog audio signals in response to a system controlling section 40. An output of the auxiliary input selector 85 is sent to an A/D converter 11.

A digital audio input signal from a terminal 20, specified by a standard (IEC-958) of a digital audio interface in the IEC standards, is applied to the digital input decoder 21 for producing digital input, sub-code, and synchronizing signals. An output signal of the digital input decoder 21, i.e., sub-code data is sent to a digital copy control signal detection circuit 22 for detecting a digital copy control signal included in the sub-code signal. The synchronizing signal is sent to a synchronizing error detection circuit 24 for detecting errors in bit synchronizing or frame synchronizing by comparison between said synchronizing signal and a reference synchronizing signal.

An output of the A/D converter 11 is sent to "d" input of a record signal selector 30 through a polarity changing circuit 81 mentioned latter. Another input "c" of the record signal selector 30 is supplied with an output of the digital input decoder. The record signal selector 30 selects either the output signal of the A/D converter 11 or the output signal of the digital input decoder 21, i.e., digital data. An output signal of the record signal selector 30 is recorded on a magnetic tape 54 through a record signal processing circuit 50 for formatting the audio digital signal for recording together with sub-code from a sub-code encoder 51, through a recording circuit 52, and through a head 53. The digital copy control signal detected by the digital copy control signal detection circuit 22 is sent to a system controlling section 400.

The polarity changing circuit 81 changes polarity of the output signal of the A/D converter 11. It changes polarity relation between the output of the A/D converter 11 and the digital data. Numeral 84 is a signal correlation detection circuit for detection

difference between the output of A/D converter and the digital data in polarity, magnitude, and phase for generating a polarity control signal 841 and correlation detection signal 844.

The system controlling section 40 comprises a microprocessor (mpu) for controlling the whole system through communication through its input and output ports with peripheral circuits and logical calculation processing therein. As structure of the microprocessor (mpu) is well-known, thus, the detailed description is omitted. Fig. 2 shows a flow chart showing flows of controlling operation of the first embodiment which is common to embodiments through the specification. A program stored in the system controlling section 40 is provided such that the system controlling section 40 operates in accordance with the flow chart of Fig. 2. Numeral 41 included in the system controlling section 40 is a permission/inhibition determination section for making determination as to permission/inhibition of digital copying in accordance with the digital copy controlling and synchronizing error detection signals. Numeral 42 is a digital copying recording controlling signal generation section included in the system controlling section for generating a digital controlling signal to be recorded on the recording medium. Numeral 51 is a sub-code encoder for converting the digital copy controlling signal into a sub-code formatted signal. Actually, the mpu executes a program of flow chart in Fig. 2 for performing functions of the digital copy permission/inhibition determination section 41; digital copy recording control signal generation section 42, and the operation mode controlling section 43. Numeral 60 is a operation switch. Numeral 70 is an indicator.

Hereinbelow will be described operation of digital copying in the above-mentioned data recording apparatus.

When an operator sets the apparatus to be in the digital copy mode with the operation switch 60 (step 102), the system controlling section 40 sends a control signal to the auxiliary input selector 85 so that the auxiliary input selector 85 selects a signal coming from the auxiliary analog input terminal 90 (step 121). Moreover, the system controlling section 40 controls the record signal selector 30 to select the digital input signal (step 121). Then, the system controlling section 40 detects outputs of the digital copy control signal detection circuit 22 and the synchronizing error detection circuit 24 (step 103) to determine synchronizing condition and permission/inhibition of digital copying (step 104). If the answer is "permission", the system controlling section 40 turns the recording circuits into recording condition (step 105). If the answer is "inhibition", processing proceeds to step 122 where the system controlling section 40 checks an output of the signal correlation detection circuit 84 to detect correlation (step 123). If there is correlation, it controls the recording signal selector 30 to change signal selection from the digital input to the analog input signal. Thus, the signal being recorded is switched to the signal from the auxiliary analog input terminal 90 (step 112). In addition to this operation, indications of substitution recording is executed in step 112, as well as information whether there is synchronizing error or not and digital copying is permitted or inhibited is made by the indicator 70 to arouse the operator's attention. Therefore, even if the apparatus is set to the digital copying mode, it can record the input signal coming from the auxiliary analog input terminal 90, converted into a digital signal by through the A/D converter 11.

Fig. 3 shows interconnection between this apparatus and an external apparatus, which is suited for embodiments throughout the specification. In Fig. 3, numeral 1a, 1b, 1c, 1d, or 1e is a DAT. Numeral 4 is a CD player. Numeral 410 is an analog signal output terminal. Numeral 420 is a digital signal output terminal. The DAT is connected to the CD player, as shown in Fig. 3. Thus, both the auxiliary analog input terminal 90 and the digital signal input terminal 20 are supplied with a reproduction signal of the same CD player. Therefore, when synchronizing error or inhibition of digital copy occurs, the apparatus detects synchronizing error and inhibition of digital copy and thus, it can record the analog signal automatically in replace with the digital signal.

Other flows of the flow chart in Fig. 2 will be described.

After starting recording (step 105) with the digital input selected, the apparatus executes detection of synchronizing error and of digital copy control signal (steps 107 and 109). If synchronizing is in not error and the digital copy control signal indicates permission of copy, the apparatus maintains digital copying operation (step 111). If synchronizing is in error or the digital copy control signal indicates inhibition of digital copy (step 108), processing proceeds to step 122 where correlation is determined with the output of the signal correlation detection circuit 84 (step 123). If there is correlation, the system controlling section 40 controls the recording signal selector 30 to change signal selection from the digital input to the analog input. Even though once the apparatus is in digital copy mode, the apparatus can record the signal inputted to the auxiliary analog input terminal 90 converted into digital signal by the A/D converter 11. If the apparatus is interconnected as shown in Fig. 3 and when synchronizing error or inhibition of copy during recording the digital signal, it can record the analog signal in stead of the digital input

signal automatically in response to detecting such conditions.

Moreover, analog input recording of step 112 is included in the loop of detecting the condition of the digital input decoder, so that when synchronising error is recovered or inhibition is cancelled, the apparatus can return to the original state, i.e., the digital input recording condition (step 111). In this respect, this technique is different from the original analog input selection recording (step 113). After recovering of error or cancel of inhibition, the apparatus can returns automatically to the digital copying operation whose sound quality is not deteriorated. Thus, the whole content of the program can be recorded though the digital control signal turns into inhibition of digital copying during recording when using the audio signal from a magnetic tape where the number of generations of possible digital copying is specified. This is because a portion of the content where digital copying is not permitted can be recorded using a signal from the auxiliary analog input terminal 90 via analog circuits. Thus, the problem that a muted signal is recorded in the recorded tape can be removed. Similarly, in the case of synchronizing error, the problem that recording is interrupted or a muted portion is made, is removed. Moreover, in step 112, it is possible to indicate of impossibility of digital copy and to further indicate whether synchronizing error or inhibition digital copying causes the impossibility. Thus, the operator can know the condition from these indications, so that the indication promotes a recovering operation against the trouble when synchronization error occurs.

Fig. 4 is a block diagram of the polarity changing circuit 81. In Fig. 4, the polarity changing circuit 81 comprises n EXCLUSIVE OR gates 81-1 to 81-n whose one inputs are supplied with the output of the A/D converter 11 respectively, as shown in Fig. 4. Another inputs of the EXCLUSIVE OR gates are supplied with the polarity control signal 841 from the signal correlation detection circuit 84. The output of the EXCLUSIVE OR gates 81-1 to 81-n are sent sto the record signal selector 30. Therefore, the polarity changing circuit changes polarity of the output of the A/D converter 11 in response to the polarity signal from the signal correlation detection circuit 84.

Fig. 5A is a block diagram of the signal correlation circuit 84. In Fig. 5A, the output 845 of the polarity changing circuit 81 is applied to a peak detector circuit 89a. The output of the digital input decoder is applied to another peak detector 89b. The most significant bit MSB of the output 845 is also applied to one input of an EXCLUSIVE OR gate 85 of a circuit 84a. Another input of the EXCLUSIVE OR gate 85 is supplied with the MSB of the output 846. An output of the EXCLUSIVE OR 85 is sent to an integrator 86. An output of the integrator 86 is supplied to comparators 87 and 88. The comparators 87 and 88 are supplied with reference signals REF1 and REF2 respectively. One output 841 of the circuit 84a, i.e., the polarity signal from the comparator 87 detects consistency of polarity between the outputs 845 and 846. The polarity changing circuit 81 changes polarity of its output signal in response to the polarity signal 841 to consist polarity of its output with the output of the digital decoder 21. On the other hand, another output 844 of the circuit 84a from the comparator 88 shows correlation between the outputs 845 and 846. This is because if there is correlation of opposite polarity between outputs 845 and 846, at first, the comparator detects polarity difference and the polarity changing circuit 81 changes its polarity. Then, the comparator 88 can detect whether there is correlation between the outputs 845 and 846 or there is no correlation. If there is correlation of the same polarity between outputs 845 and 846, the comparator 88 can detect whether signal correlation exist or not at once. However, there are many techniques for detecting signal correlation and it is possible to detect correlation of the same polarity and the opposite polarity at once.

The peak detector 89a detects peak time and peak value of the output 845 to produce a peak time pulse and peak data respectively. The peak detector 89b detects peak time and peak value of the output 846 to produce a peak time pulse and peak data respectively. The peak time pulses are applied to a time difference detector 91 which detects time difference between peaks of the outputs 845 and 846. Fig. 5B shows a block diagram of the peak detectors 89a and 89b. In Fig. 5B, output 845 or 846 is supplied to n EXCLUSIVE OR gates 94 as shown, which detects an absolute value. The absolute value is sent to inputs of digital comparator 96 and D latch array 95. Another inputs of the digital comparator 96 are supplied with a Q outputs of the D latch array 95. An output of the digital comparator 96 shows the peak time pulse. The Q output of the D latch array 95 shows the peak data. A reset input of the D latch 95 is supplied with a clock signal CLK 1 for detecting the peak time pulse and the peak data within a given interval. Fig. 5C is a block diagram of the time difference detector 91. The peak time pulse from the peak detector 89a is applied to a reset input of a counter 97 whose clock pulse input is supplied with a clock CLK2. Thus, the counter starts counting in response to the peak time pulse of the peak detector 89a. An output of the counter 97 is sent to a D latch 99 whose clock pulse input is supplied with the peak time pulse from the peak time detector 89b. Thus, a Q output of the D latch 99 holds a data of the output of the counter 97 in response to

the peak time pulse from the peak detector 89a. This data shows time difference between the peaks of the outputs 845 and 846.

The signal correlation signal 844 shows the signal correlation between the analog signal and the digital input signal correctly after the polarity control signal 841 is produced. Thus, the mpu 40 detects the signal correlation signal with a delay time after switching the record signal selector 30.

Hereinbelow will be described a second embodiment of the data recording apparatus of the invention with reference to drawings. Fig. 6 is a block diagram showing the second embodiment of the invention. Fig. 2 shows a flow chart showing controlling operation of the second embodiment also. In Fig. 6, the basic structure of the second embodiment of Fig.6 is the same as that of the first embodiment. Different points are that a variable delay circuit 82 is provided between the A/D converter 11 and the record signal selector 30, a delay circuit 182 is provided between the digital input decoder 21 and the record signal selector 30, and the polarity changing circuit 81 is omitted. Therefore, a detailed description will be omitted and different points are described mainly. The variable delay circuit 82 delays the signal from the analog input by a delay time determined by the delay control signal 842. The delay circuit 182 delays the digital audio signal from the digital decoder 21 by a given delay time. Operation of digital copying of the data recording apparatus structured as mentioned above will be described, particularly, operation of the variable delay circuit 82 will be described mainly, which is a different point from the first embodiment.

The signal correlation detection circuit 84 detects, for a given interval, time difference between an instance when the output signal of the A/D converter 11 reaches a peak value in amplitude and another instance when the output signal of the digital input decoder 21 reaches a peak value in amplitude. The signal correlation detection circuit 84 sends a delay control signal 842 to the variable delay circuit 82 in accordance with the detection signal. That is, it control a delay time of the output signal of the A/D converter 11 such that both the signal of the A/D converter 11 and the output signal of delay circuit 182 reaches the record signal selection circuit 30 at the same instance. Therefore, the unnatural variation in the output level of the record signal selection circuit 30 due to change of signal selection can be reduced. Generally, amount of delay for the analog signal is longer than that of the digital signal because there is large delay at a filter for removing distortion. Therefore, the delay circuit 182 is provided in the digital input signal line and the variable delay circuit 82 is provided in the output line of the A/D converter 11 to control delay time for time-adjusting between the digital and analog input signals. However, in order to ensure that the digital audio signal reaches the record signal selector 30 earlier than the analog audio signal, only the variable delay circuit 82 may be provided between the A/D converter 11 and the record signal selector 30.

At start of the operation the delay amount of the variable delay circuit 82 is set to the max by the delay control signal 842 to prevent that the analog audio signal reach to the record signal selector 30 earlier than the digital audio signal.

Hereinbelow will be described a third embodiment of the data recording apparatus of the invention with reference to drawings. Fig. 7 is a block diagram showing the third embodiment of the invention of data recording apparatus. Fig. 2 shows a flow chart shoring controlling operation of the third embodiment of Fig. 7 also. In Fig. 7, the basic structure of the third embodiment of Fig. 7 is the same as that of the first embodiment. Different points are a variable gain amplifier 83 is provided between the input terminal 90 and the input selector 85 and the polarity changing circuit 81 is omitted. Therefore, a detailed description will be omitted and different points are described mainly. The variable gain amplifier 83 changes gain for the analog input signal in accordance with a gain control signal 843. Operation of digital copying of the data recording apparatus structured as mentioned above will be described, particularly, operation of the variable gain amplifier will be described mainly, which is a different point from the first embodiment. The signal correlation detection circuit 84 detects peak values of the output signal of the A/D converter 11 and the output signal of the digital input decoder 21 for a given interval and compares them and detects deference in amplitude of these signals. The signal correlation detection circuit 84 sends a gain control signal 843 to the variable gain amplifier 83 in accordance with the detection result. That is, it control amplitude of the log input signal such that amplitudes of the output signal of the A/D converter 11 is made substantially equal to that of the output signal of digital signal decoder 21. Therefore, the unnatural variation in the output level of the record signal selector 30 due to change of signal selection can be reduced.

Hereinbelow will be described a fourth embodiment of the data recording apparatus of the invention with reference to drawings. Fig. 8 is a block diagram showing the fourth embodiment of the invention of data recording apparatus. Fig. 2 shows a flow chart showing controlling operation of the fourth embodiment of Fig. 8. In Fig. 8, the basic structure of the fourth embodiment of Fig. 8 is the same as that of the first embodiment. Different points are that a variable delay circuit 82 and

variable gain amplifier 83 are provided. Therefore, a detailed description will be omitted. Operation of digital copying of the data recording apparatus structured as mentioned above will be described. In the fourth embodiment, in order to increase signal correlation, there are provided the polarity changing circuit 81, variable delay circuit 82 and variable gain circuit 83. The signal correlation detection circuit 84 supplies polarity control signal 841, delay control signal 842, and gain control signal 843 to control adaptively these circuits. Thus, it is possible to make the output signal of the A/D converter 11 substantially equal to the output signal of the A/D converter 21 in amplitude and in phase (delay and polarity) at the input of the record signal selector 30. Therefore, an unnatural variation in the output level of the record signal selector 30 at an instance that signal selection is changed can be reduced.

Hereinbelow will be described a fifth embodiment of the data recording apparatus of the invention with reference to drawings. Fig. 9 is a block diagram showing the fifth embodiment of the invention of data recording apparatus. Fig. 2 shows a flow chart showing controlling operation of the fifth embodiment of Fig. 9 also. In Fig. 9, the basic structure of the fifth embodiment of Fig. 9 is the same as that of the fourth embodiment. A different point is that a muting circuit 31 are provided. Therefore, a detailed description will be omitted. The muting circuit 31 replaces the record signal with a muted signal in accordance with the control signal of the system control circuit 40. Operation different from other embodiments of the data recording apparatus as structured as mentioned above for digital copy will be described. In step 122, these system control circuit 40 checks the output of the signal correlation detection circuit 84 (step 123). If it judges the output as not in correlation, it controls the muting circuit 31 so that a muted signal is recorded (step 124). That is, if the signal inputted into the auxiliary analog signal input terminal 90 is different from that inputted into the digital signal input terminal 20, it controls the muting circuit 31 to record the muted signal during these signals being inconsistent with each other. Thus, a problem that a desired program is recorded on the magnetic tape 54 with other program mixed together. In step 124, in addition to this, an indication showing muted signal being recorded is made to show that substitution recording with the analog signal is not permitted or there is a problem. The operator can tray again recording or can check digital signal lines or the auxiliary analog input lines. Thus, if there is no correlation, such error condition is indicated as well as a problem that a desired program is recorded with other program mixed.

Moreover, other operation in addition to embodiments mentioned above. When the magnetic tape 54 recorded in the way of each embodiment is reproduced, a sub-cord is recorded on the magnetic tape 54 because it is desired that a portion of the magnetic tape where analog recording is carried out can be distinct from another portion where digital recording is carried out. Actually, the operation mode controlling circuit 43 receives a result from the digital copy permission/forbidden detection circuit 41 and sends it to the digital copy control signal for recording generation circuit 42. Then the result is converted into a sub-cord format data by the sub-code encoder 51 to supply it to the record signal processing circuit 50. The record signal processing circuit 50 produces a record signal using the main data together with the sub-cord data in accordance with a record format. The record signal is recorded by the head 53 on the magnetic tape through the recording circuit. Therefore, when the recorded tape is reproduced it is possible to distinguish the portion where analog signal is recorded from another portion where digital signal is recorded. This can be utilized for indication. Such indication provides the operator history of the magnetic tape with respect to copying, so that it gives the operator useful information for operating and maintenance of the system and it removes an feeling of uneasiness and a suspicion during operation.

In the above-mentioned embodiments, the system controlling is carried out using both data of the synchronizing error detection from the digital input decoder 21 and copying inhibition bit from the digital copy control signal detection circuit 22. However, only either data from the synchronizing error detection circuit or from the digital copy control signal detection circuit 22 can be used for controlling, as clearly shown from the above-mentioned description. Each data occurs separately and has each function and effect.

This invention is not limited to a scope of the DAT, but is widely applicable to data recording apparatus for being capable of recording either analog or digital signal, for example, digital video tape recorder, AV disc recorder, or digital solid-state memory recorder, etc.

Claims

1. A data recording apparatus comprising;
   (a) an A/D converter for converting an analog input signal;
   (b) a digital decoder for decoding a digital input signal to obtain digital data and a synchronizing signal;
   (c) selecting means responsive to a control sig-

nal for selecting either an output of the A/D converter or said digital data for recording;

(d) synchronizing error detection means for detecting synchronizing error through comparison between said synchronizing signal and a reference synchronizing signal; and

(e) control means responsive to an output of said synchronizing error detection means for producing said control signal to cause said selecting means to select said output of said A/D converter when synchronizing error is detected.

2. A data recording apparatus as claimed in Claim 1, wherein said control means produces the control signal in response to said output of said synchronizing error detection means to cause said selecting means to select said digital data when synchronizing error is removed.

3. A data recording apparatus comprising;

(a) an A/D converter for converting an analog input signal;

(b) a digital decoder for decoding digital input signal to obtain a digital data and a sub-code signal;

(c) selecting means for selecting either an output of the A/D converter or said digital data in response to a control signal;

(c) detection means responsive to said sub-code signal for detecting a copy control signal indicative of permission and inhibition of recording with said digital input signal; and

(d) control means responsive to said detected copy control signal for producing said control signal to cause said selecting means to select said output of said A/D converter when said inhibition is detected.

4. A data recording apparatus as claimed in Claim 3, wherein said control means produces said control signal in response to said detected copy control signal to cause said selection means to select said digital data when said detected copy control signal indicates said permission.

5. A data recording apparatus as claimed in Claim 1, further comprising:

(a) polarity difference detection means for detecting polarity difference between said output of said polarity changing means and said digital data, and

(b) polarity changing means for changing polarity of said output of A/D converter in response to an output of said polarity difference detection means.

6. A data recording apparatus as claimed in Claim 3, further comprising:

(a) polarity difference detection means for detecting polarity difference between said output of said polarity changing means and said digital data, and

(b) polarity changing means for changing polarity of said output of A/D converter in response to an output of said polarity difference detection means.

7. A data recording apparatus as claimed in Claim 1, further comprising:

(a) phase difference detection means for detecting phase difference between said output of said A/D converter and said digital data; and

(b) time-adjusting means for adjusting time difference between said output of said A/D converter and said digital data in response to an output of said phase difference detection means.

8. A data recording apparatus as claimed in Claim 7, wherein said phase difference detection means comprises:

(a) first peak instant detecting means for detecting instance of a first peak of said output of said A/D converter for a given interval;

(b) second peak instant detecting means for detecting instant of a second peak of said digital data for said given interval; and

(c) time difference measuring means responsive to said detected instant of said first and second peak for producing said output of said phase difference detection means by measuring time difference therebetween.

9. A data recording apparatus as claimed in Claim 3, further comprising:

(a) phase difference detection means for detecting phase difference between said output of said A/D converter and said digital data; and

(b) time-adjusting means for adjusting time difference between said output of said A/D converter and said digital data in response to an output of said phase difference detection means.

10. A data recording apparatus as claimed in Claim 9, wherein said phase difference detection means comprises:

(a) first peak instant detecting means for detecting instance of a first peak of said output of said A/D converter for a given interval;

(b) second peak instant detecting means for detecting instant of a second peak of said digital data for said given interval; and

(c) time difference measuring means responsive to said detected instant of said first and second peak for producing said output of said phase difference detection means by measuring time difference therebetween.

11. A data recording apparatus as claimed in Claim 1, further comprising:

(a) peak difference detection means for detecting peak value difference between said output of said A/D converter and said digital data; and

(b) variable gain amplifier for amplifying said analog input with a gain determined by an output of said peak difference detection means.

12. A data recording apparatus as claimed in Claim

11. wherein said peak difference detection means comprises:

(a) first peak detecting means responsive to said output of said A/D converter for detecting peak value;

(b) second peak time detecting means responsive to said digital data; and

(c) a subtractor responsive to said first and second peak detecting means for producing said output of said peak difference detection means by subtracting.

13. A data recording apparatus as claimed in Claim 3, further comprising:

(a) peak difference detection means for detecting peak value difference between said output of said A/D converter and said digital data; and

(b) variable gain amplifier for amplifying said analog input with a gain determined by an output of said peak difference detection means.

14. A data recording apparatus as claimed in Claim 13, wherein said peak difference detection means comprises:

(a) first peak detecting means responsive to said output of said A/D converter for detecting peak value;

(b) second peak time detecting means responsive to said digital data; and

(c) a subtractor responsive to said first and second peak detecting means for producing said output of said peak difference detection means by subtracting.

15. A data recording apparatus as claimed in Claim 1, further comprising:

second selecting means responsive to first and second analog input signals for selecting either first or second analog input signal to producing said analog input signal in response to a second control signal,

said control means producing said fifth control signal such that when said control means produces said control signal to cause said selecting means to select digital data, it produces said second control signal to cause said second selecting means to change selection between said first and second analog input signal.

16. A data recording apparatus as claimed in Claim 15, further comprising:

(a) peak difference detection means for detecting peak value difference between said output of said A/D converter and said digital data; and

(b) variable gain amplifier for amplifying said analog input with a gain determined by an output of said peak difference detection means.

17. A data recording apparatus as claimed in Claim 3, further comprising:

second selecting means responsive to first and second analog input signals for selecting either first or second analog input signal to producing said analog input signal in response to a second control signal,

said control means producing said fifth control signal such that when said control means produces said control signal to cause said selecting means to select digital data, it produces said second control signal to cause said second selecting means to change selection between said first and second analog input signal.

18. A data recording apparatus as claimed in Claim 17, further comprising:

(a) peak difference detection means for detecting peak value difference between said output of said A/D converter and said digital data; and

(b) variable gain amplifier for amplifying said analog input with a gain determined by an output of said peak difference detection means.

19. A data recording apparatus as claimed in Claim 1, further comprising:

(a) signal correlation detection means responsive to said output of said A/D converter and said digital data for detecting correlation between said output of said A/D converter and said digital data for producing a correlation signal; and

(b) muting circuit responsive to said output of said A/D converter for producing a muted signal in response to a muting control signal,

said control means producing said muting control signal when synchronizing error is detected.

20. A data recording apparatus as claimed in Claim 3, further comprising:

(a) signal correlation detection means responsive to said output of said A/D converter and said digital data for detecting correlation between said output of said A/D converter and said digital data for producing a correlation signal; and

(b) muting circuit responsive to said output of said A/D converter for producing a muted signal in response to a muting control signal,

said control means producing said muting control signal when said inhibition is detected.

FIG. 1

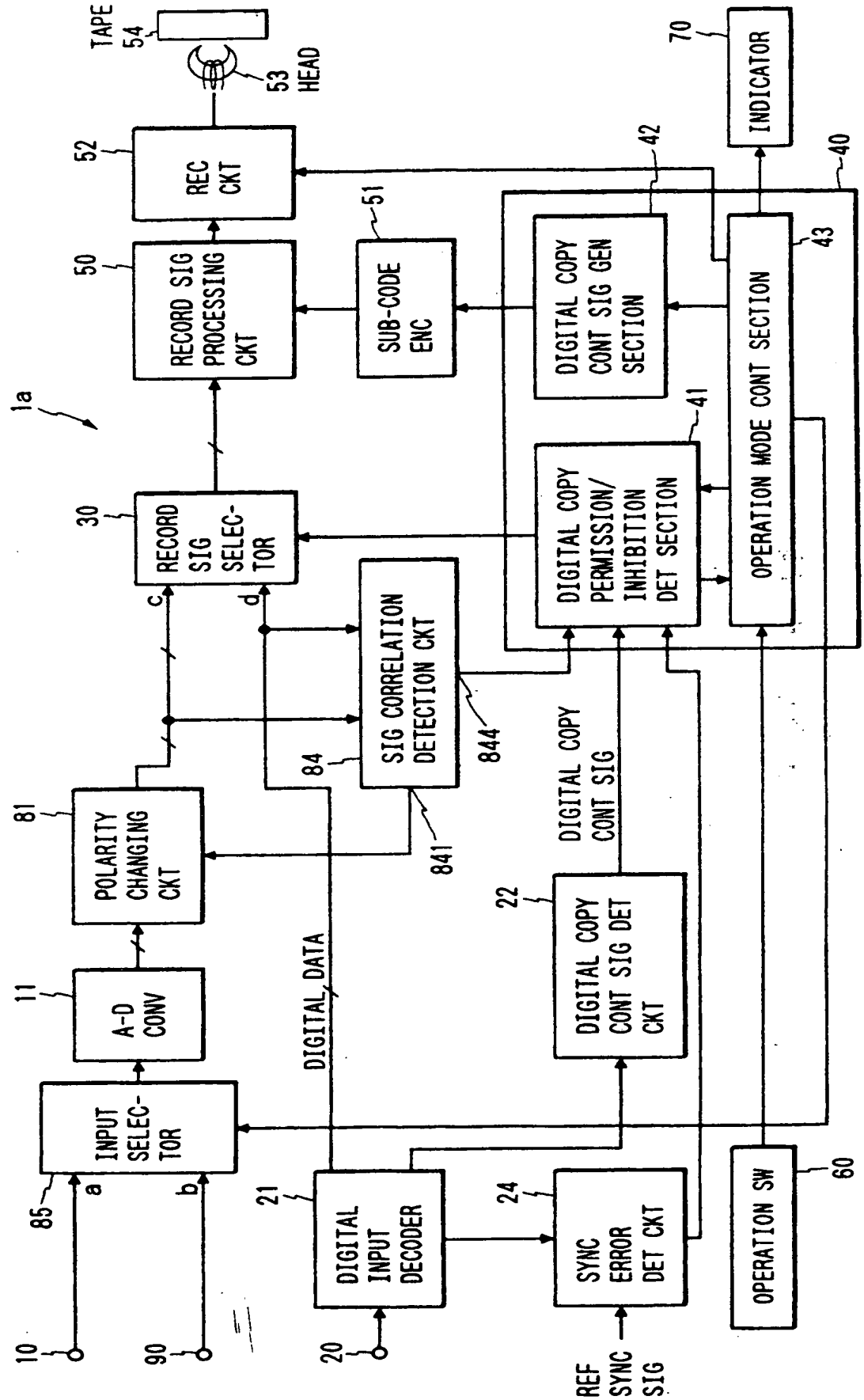

TAPE
54
53
HEAD
52
REC CKT
50
RECORD SIG PROCESSING CKT
51
SUB-CODE ENC
DIGITAL COPY CONT SIG GEN SECTION
42
70
INDICATOR
40
43
OPERATION MODE CONT SECTION
1a
30
RECORD SIG SELEC-TOR
41
DIGITAL COPY PERMISSION/ INHIBITION DET SECTION
c
d
SIG CORRELATION DETECTION CKT
844
84
81
POLARITY CHANGING CKT
841
DIGITAL COPY CONT SIG
22
DIGITAL COPY CONT SIG DET CKT
11
A-D CONV
DIGITAL DATA
INPUT SELEC-TOR
85
a
b
21
DIGITAL INPUT DECODER
24
SYNC ERROR DET CKT
OPERATION SW
60
10
90
20
REF SYNC SIG

FIG. 2

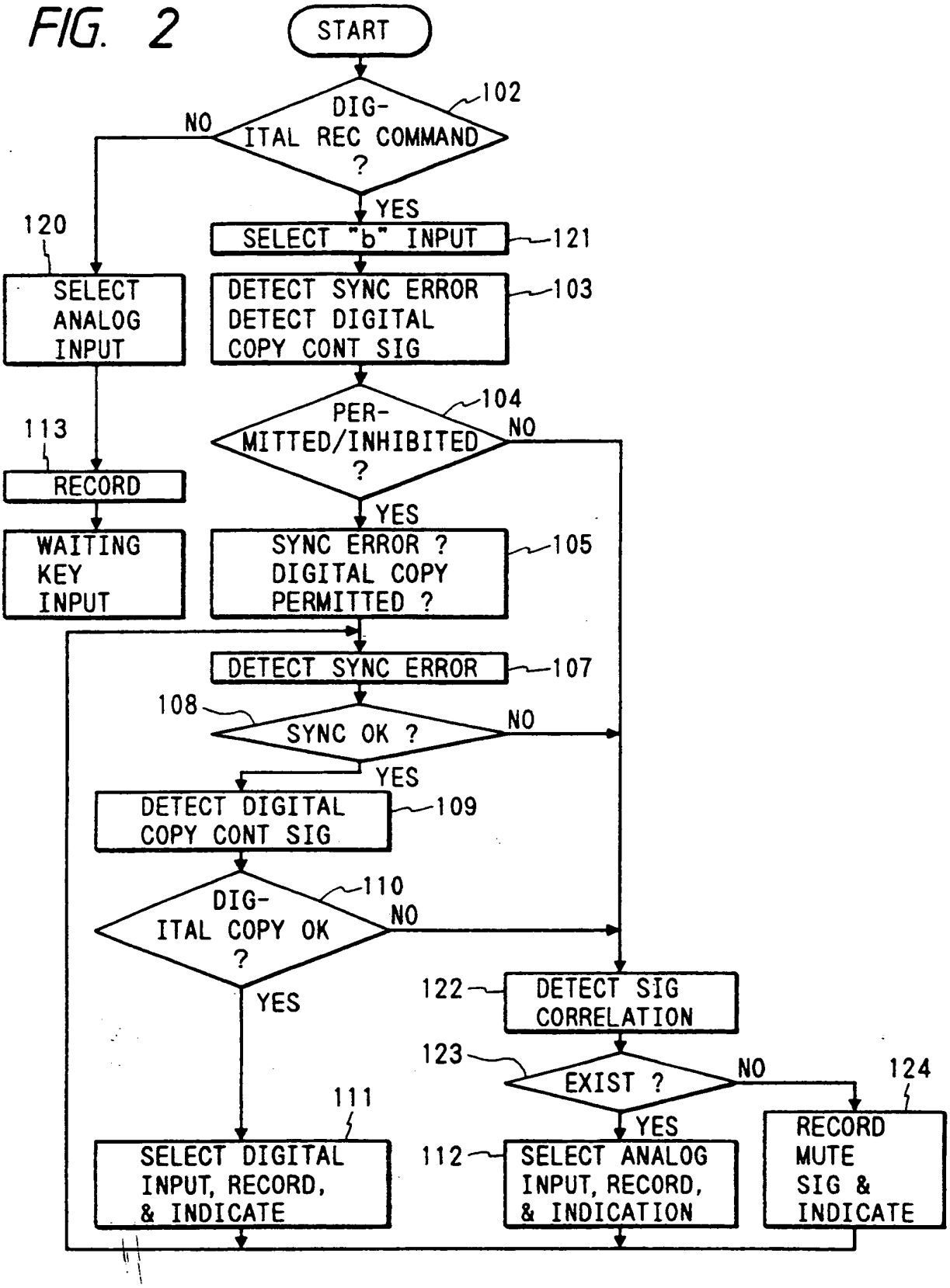

START
DIG-ITAL REC COMMAND ?
102
NO
YES
120
SELECT "b" INPUT
121
SELECT ANALOG INPUT
DETECT SYNC ERROR
DETECT DIGITAL COPY CONT SIG
103
PER-MITTED/INHIBITED ?
104
NO
113
RECORD
YES
WAITING KEY INPUT
SYNC ERROR ? DIGITAL COPY PERMITTED ?
105
DETECT SYNC ERROR
107
108
SYNC OK ?
NO
YES
DETECT DIGITAL COPY CONT SIG
109
DIG-ITAL COPY OK ?
110
NO
YES
122
DETECT SIG CORRELATION
123
EXIST ?
NO
124
YES
111
SELECT DIGITAL INPUT, RECORD, & INDICATE
112
SELECT ANALOG INPUT, RECORD, & INDICATION
RECORD MUTE SIG & INDICATE

FIG. 3

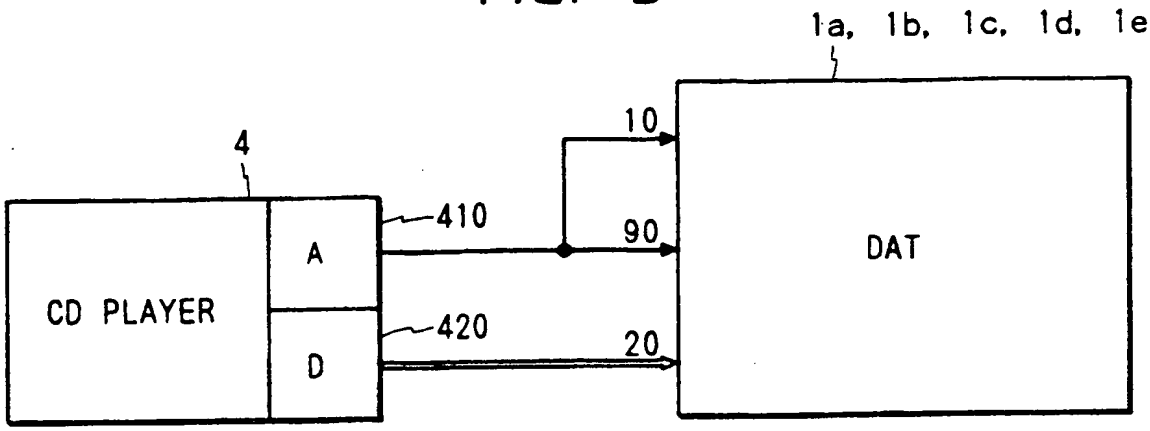

1a, 1b, 1c, 1d, 1e
4
CD PLAYER
A
D
410
420
10
90
20
DAT

FIG. 4

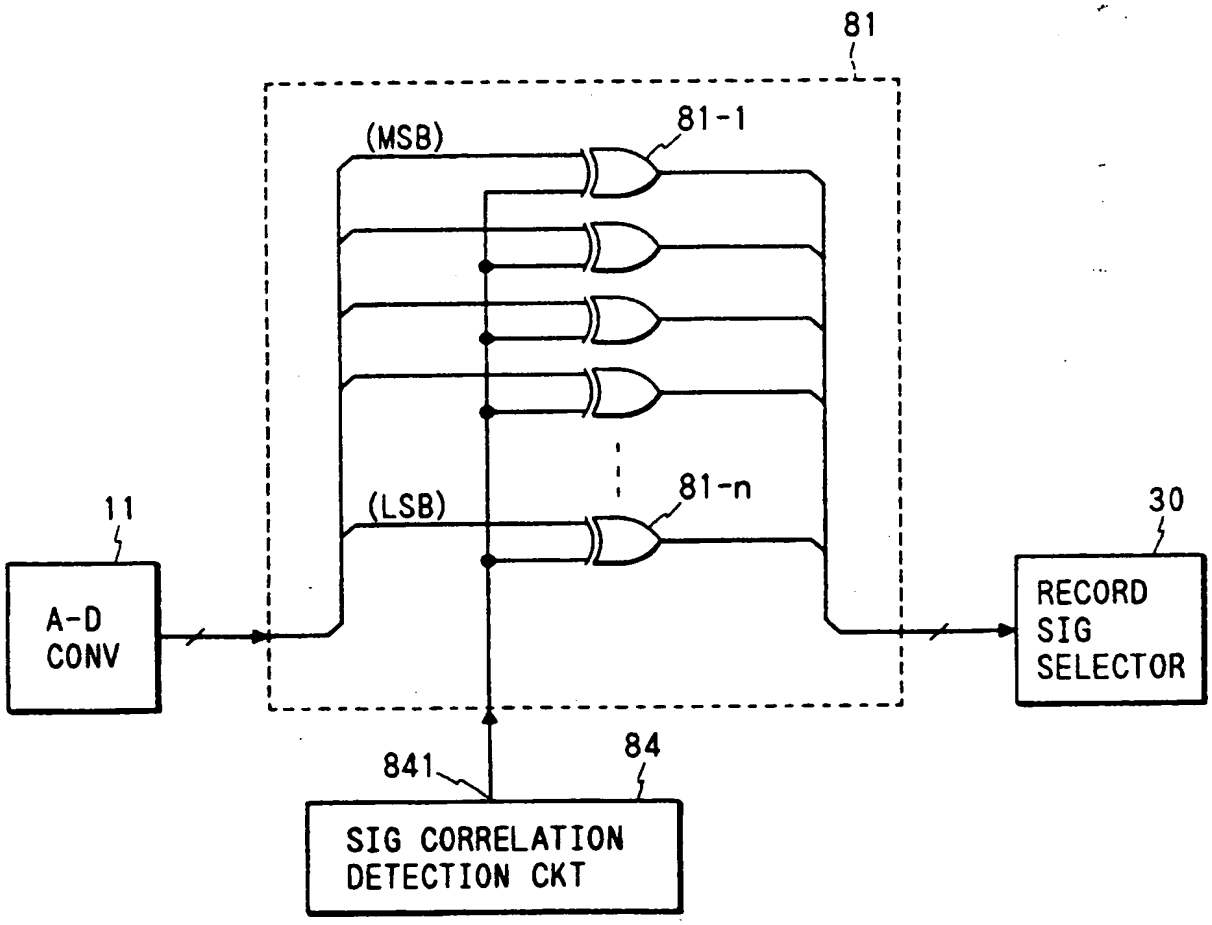

81
(MSB)
81-1
(LSB)
81-n
11
A-D CONV
30
RECORD SIG SELECTOR
841
84
SIG CORRELATION DETECTION CKT

FIG. 5A

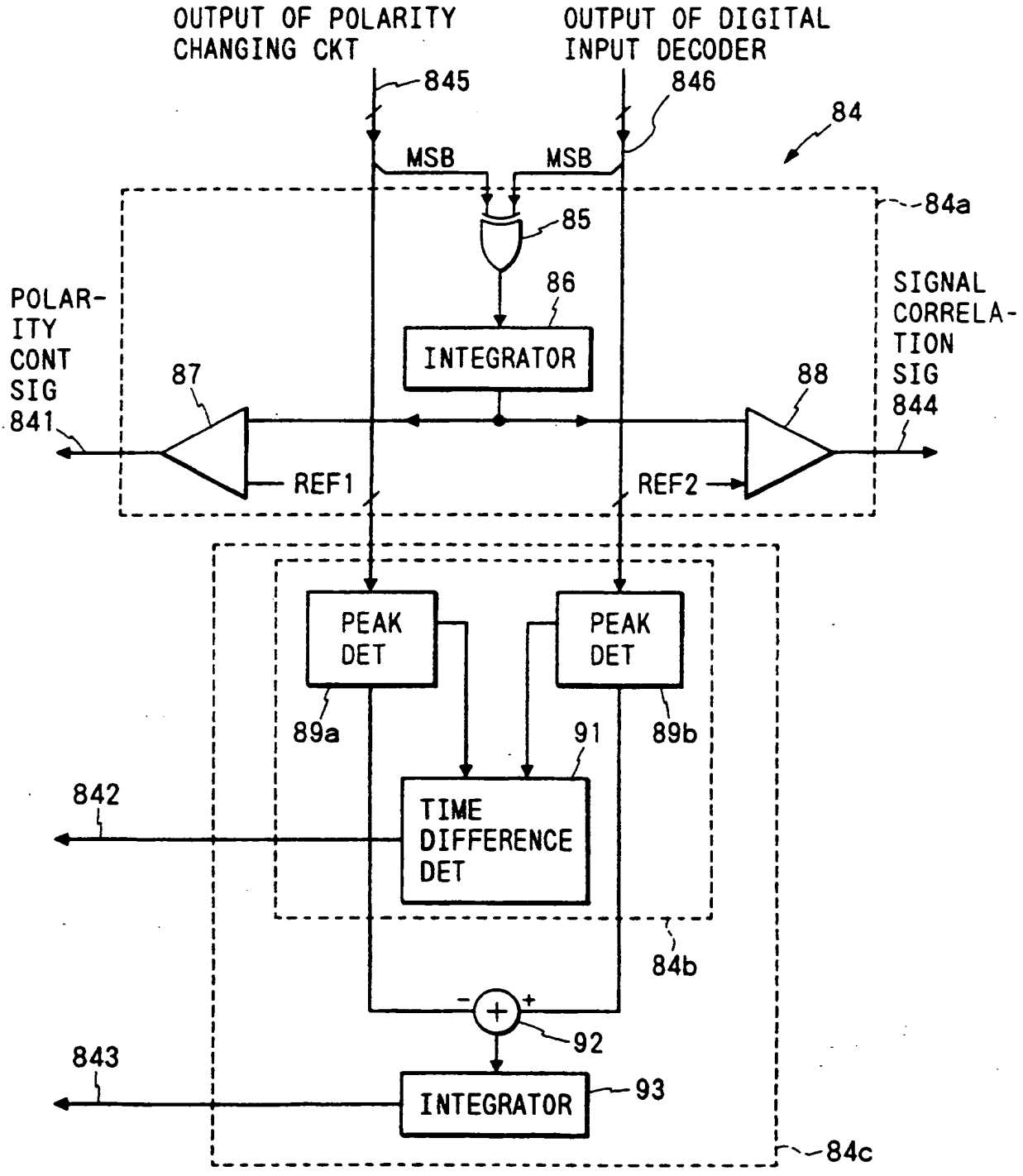

OUTPUT OF POLARITY CHANGING CKT
OUTPUT OF DIGITAL INPUT DECODER
845
846
84
MSB
MSB
84a
85
86
INTEGRATOR
POLAR-ITY CONT SIG 841
87
88
SIGNAL CORRELA-TION SIG 844
REF1
REF2
PEAK DET
PEAK DET
89a
91
89b
842
TIME DIFFERENCE DET
84b
92
843
INTEGRATOR
93
84c

FIG. 5B

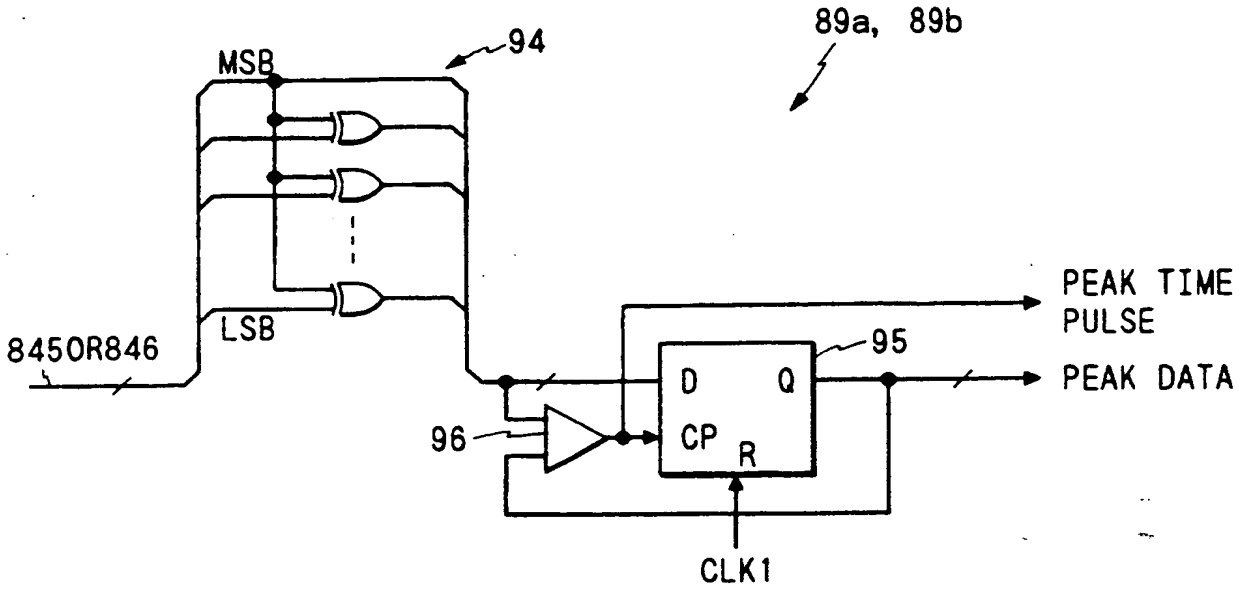

89a, 89b
94
MSB
LSB
8450R846
PEAK TIME PULSE
PEAK DATA
95
D
Q
CP
R
96
CLK1

FIG. 5C

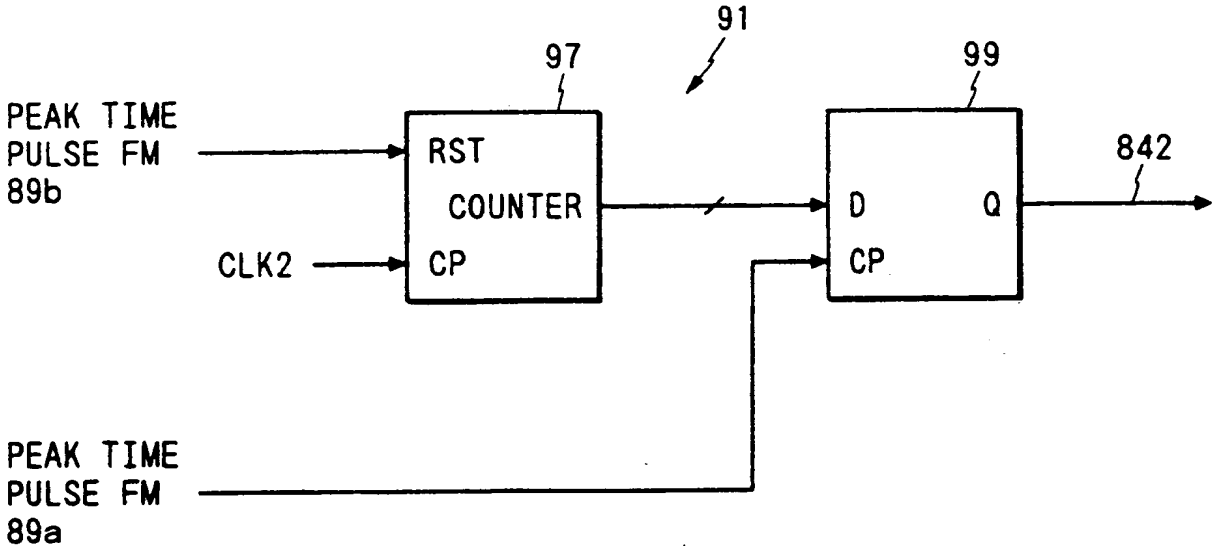

91
97
99
PEAK TIME PULSE FM 89b
RST
COUNTER
CP
CLK2
D
Q
CP
842
PEAK TIME PULSE FM 89a

FIG. 6

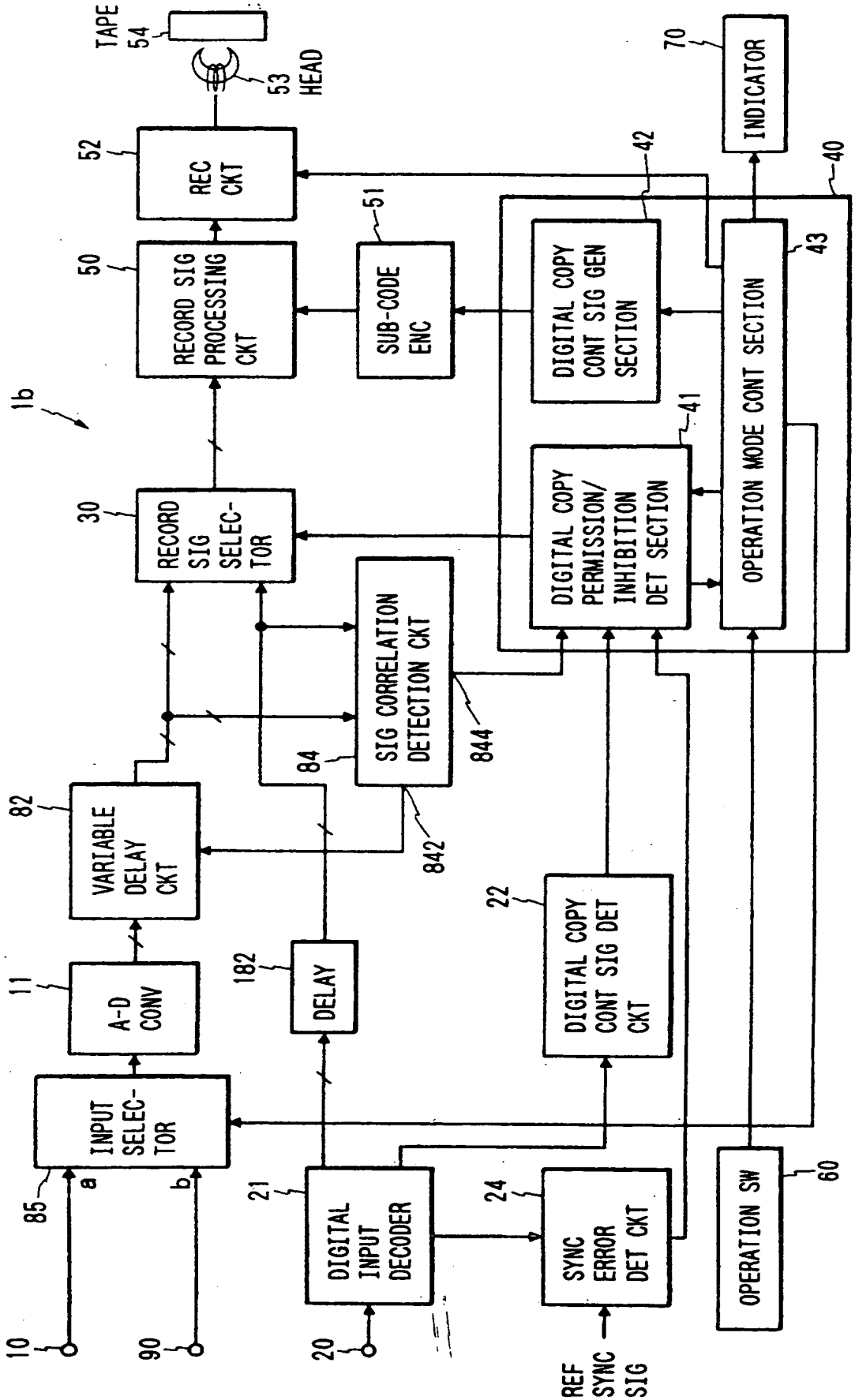

TAPE
54
53
HEAD
52
REC CKT
50
RECORD SIG PROCESSING CKT
51
SUB-CODE ENC
42
DIGITAL COPY CONT SIG GEN SECTION
70
INDICATOR
40
43
OPERATION MODE CONT SECTION
1b
30
RECORD SIG SELEC-TOR
41
DIGITAL COPY PERMISSION/ INHIBITION DET SECTION
SIG CORRELATION DETECTION CKT
844
84
842
82
VARIABLE DELAY CKT
22
DIGITAL COPY CONT SIG DET CKT
11
A-D CONV
182
DELAY
INPUT SELEC-TOR
85
a
b
21
DIGITAL INPUT DECODER
24
SYNC ERROR DET CKT
OPERATION SW
60
10
90
20
REF SYNC SIG

FIG. 7

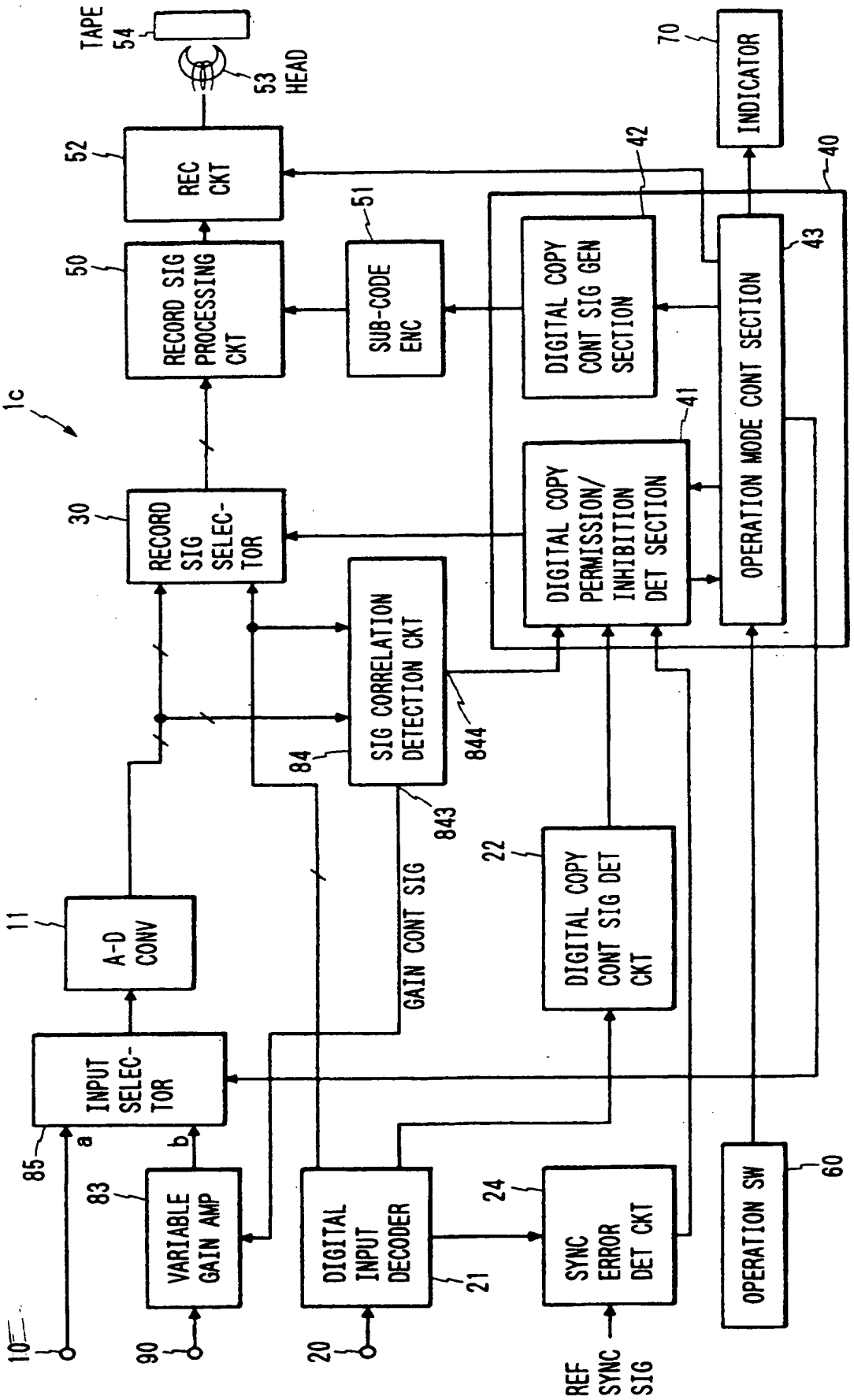

TAPE
54
53
HEAD
52
REC CKT
50
RECORD SIG PROCESSING CKT
51
SUB-CODE ENC
42
DIGITAL COPY CONT SIG GEN SECTION
70
INDICATOR
40
43
OPERATION MODE CONT SECTION
41
DIGITAL COPY PERMISSION/ INHIBITION DET SECTION
1c
30
RECORD SIG SELEC-TOR
SIG CORRELATION DETECTION CKT
844
84
843
GAIN CONT SIG
22
DIGITAL COPY CONT SIG DET CKT
11
A-D CONV
INPUT SELEC-TOR
85
a
b
83
VARIABLE GAIN AMP
DIGITAL INPUT DECODER
21
24
SYNC ERROR DET CKT
OPERATION SW
60
10
90
20
REF SYNC SIG

FIG. 8

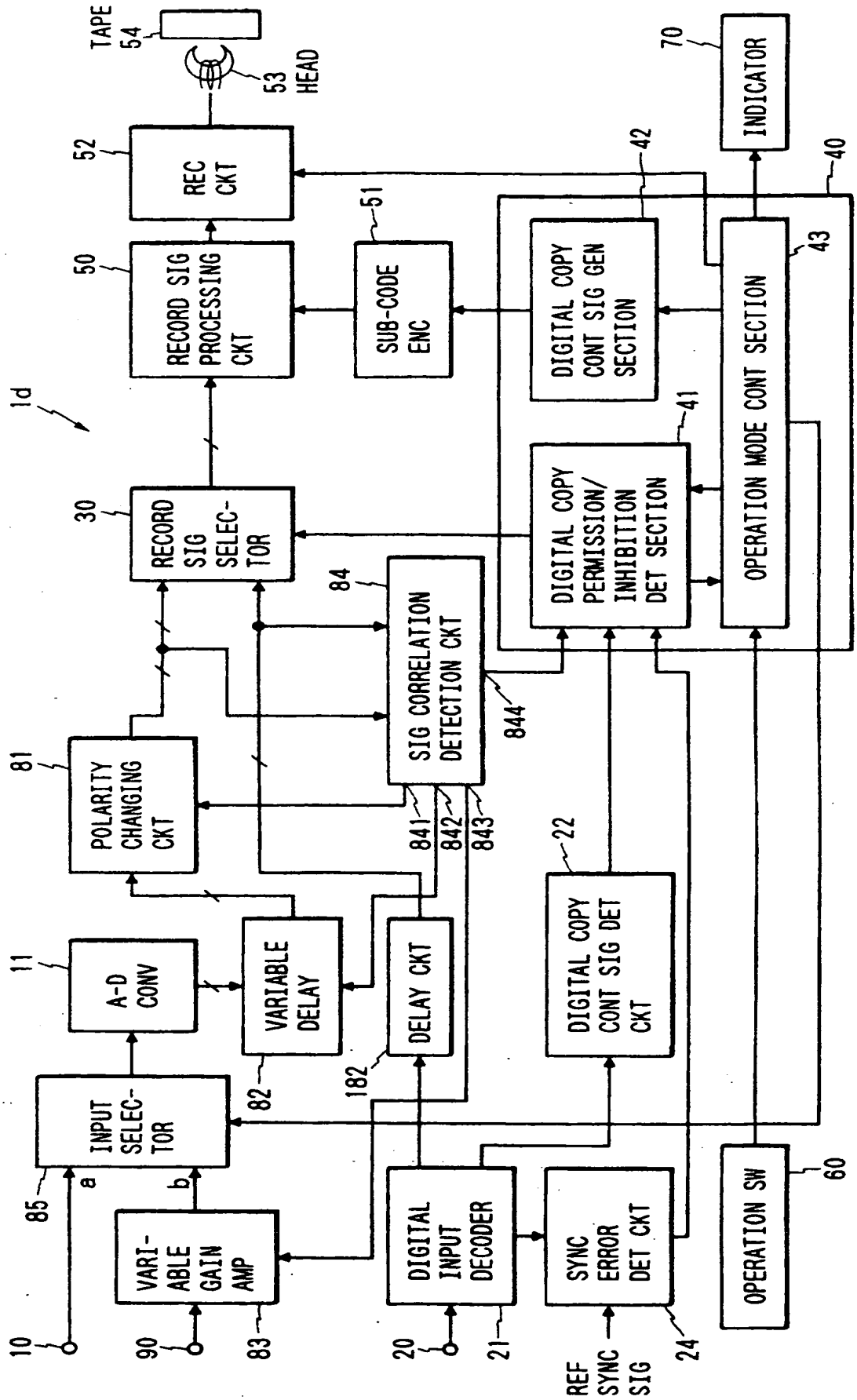
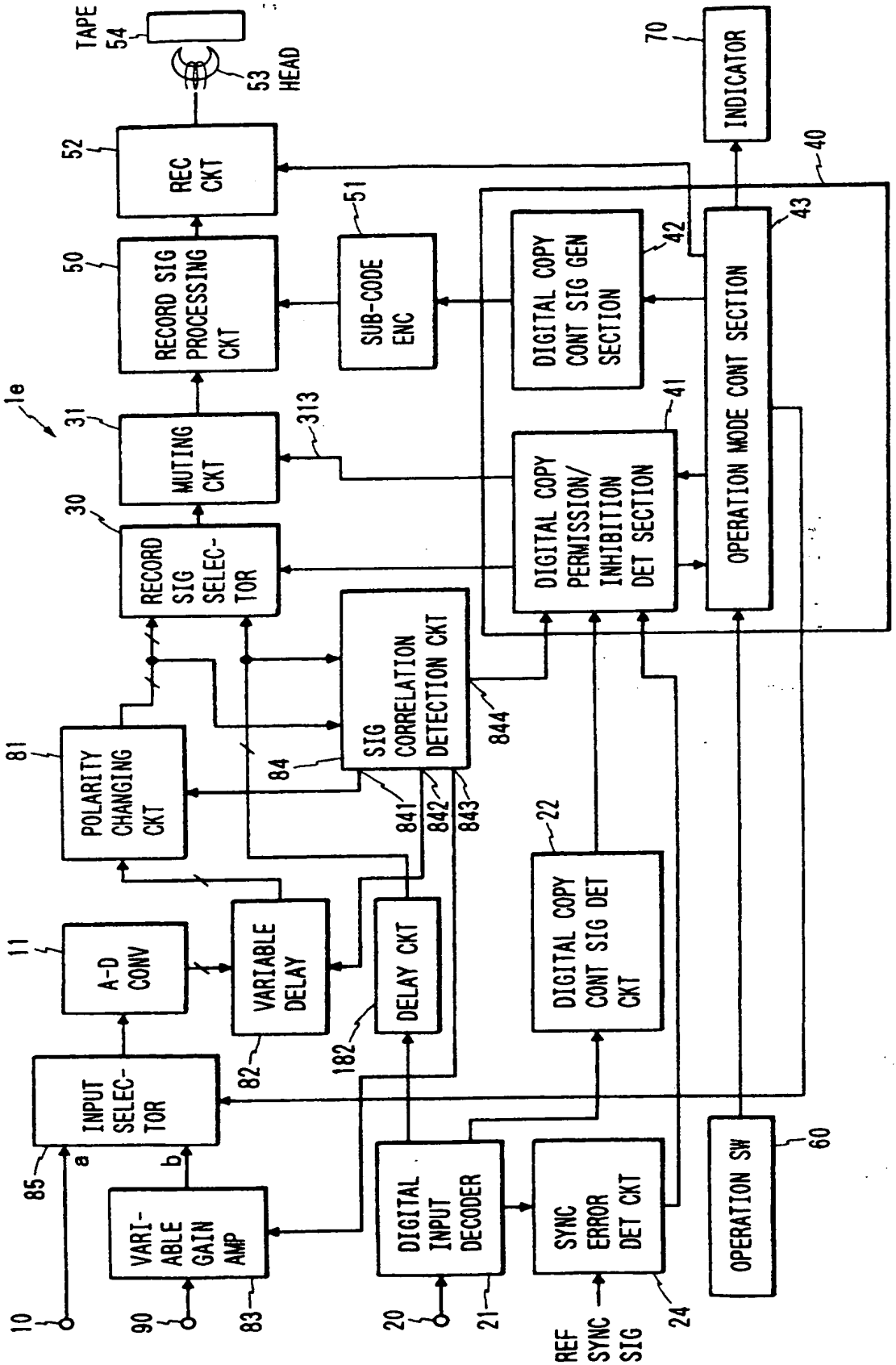

TAPE
54
53
HEAD
52
REC CKT
50
RECORD SIG PROCESSING CKT
51
SUB-CODE ENC
42
DIGITAL COPY CONT SIG GEN SECTION
70
INDICATOR
40
43
OPERATION MODE CONT SECTION
1d
30
RECORD SIG SELEC-TOR
41
DIGITAL COPY PERMISSION/ INHIBITION DET SECTION
84
SIG CORRELATION DETECTION CKT
844
81
POLARITY CHANGING CKT
841
842
843
22
DIGITAL COPY CONT SIG DET CKT
11
A-D CONV
VARIABLE DELAY
182
DELAY CKT
82
INPUT SELEC-TOR
85
a
b
VARI-ABLE GAIN AMP
DIGITAL INPUT DECODER
SYNC ERROR DET CKT
OPERATION SW
60
10
90
83
20
21
REF SYNC SIG
24

FIG. 9


TAPE
54
53
HEAD
REC CKT
52
RECORD SIG PROCESSING CKT
50
SUB-CODE ENC
51
DIGITAL COPY CONT SIG GEN SECTION
42
INDICATOR
70
OPERATION MODE CONT SECTION
43
40
1e
MUTING CKT
31
313
DIGITAL COPY PERMISSION/ INHIBITION DET SECTION
41
RECORD SIG SELEC-TOR
30
SIG CORRELATION DETECTION CKT
844
841
842
843
84
POLARITY CHANGING CKT
81
A-D CONV
11
VARIABLE DELAY
DELAY CKT
182
DIGITAL COPY CONT SIG DET CKT
22
INPUT SELEC-TOR
a
b
82
85
VARI-ABLE GAIN AMP
DIGITAL INPUT DECODER
SYNC ERROR DET CKT
OPERATION SW
60
10
90
83
20
21
REF SYNC SIG
24

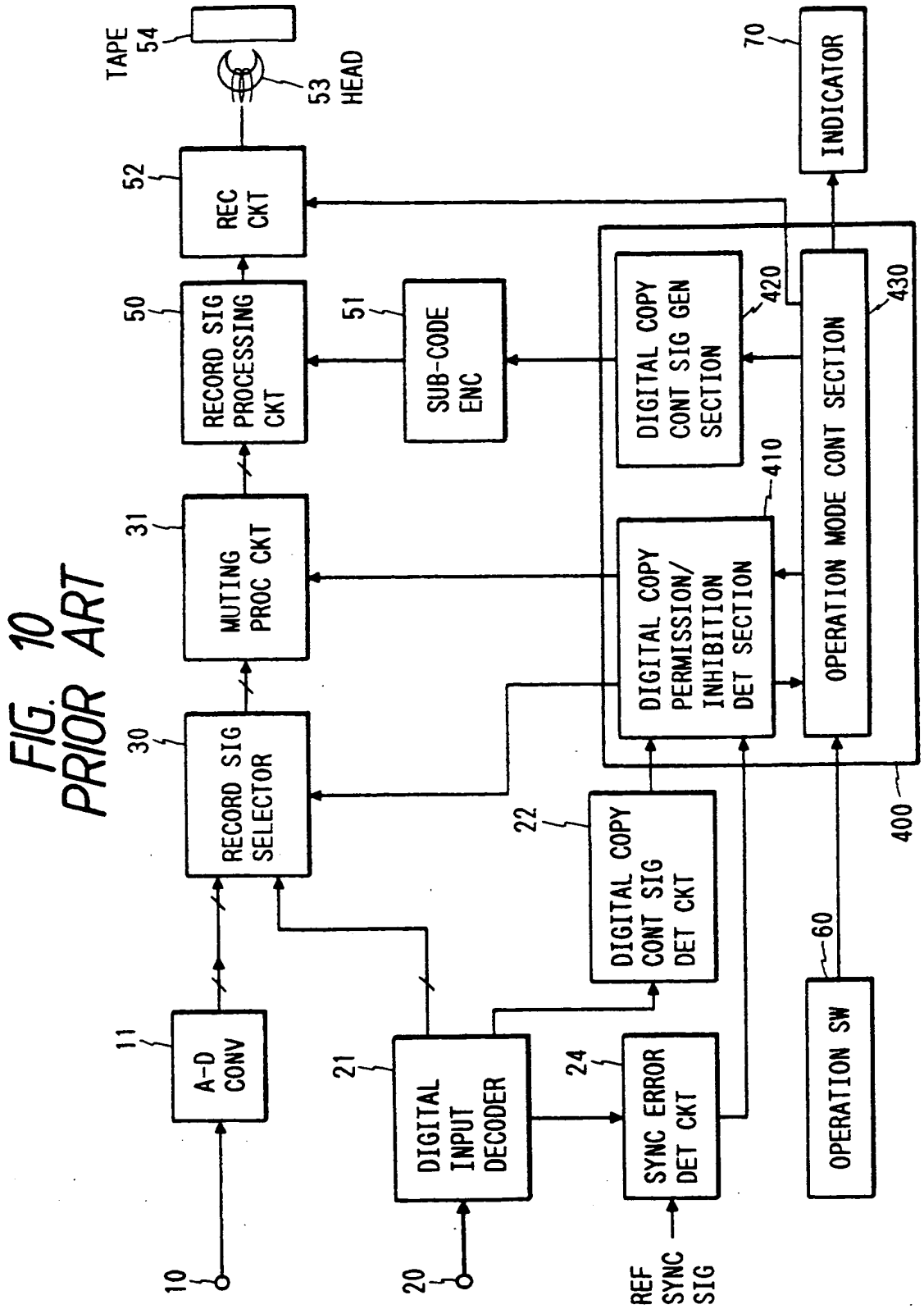
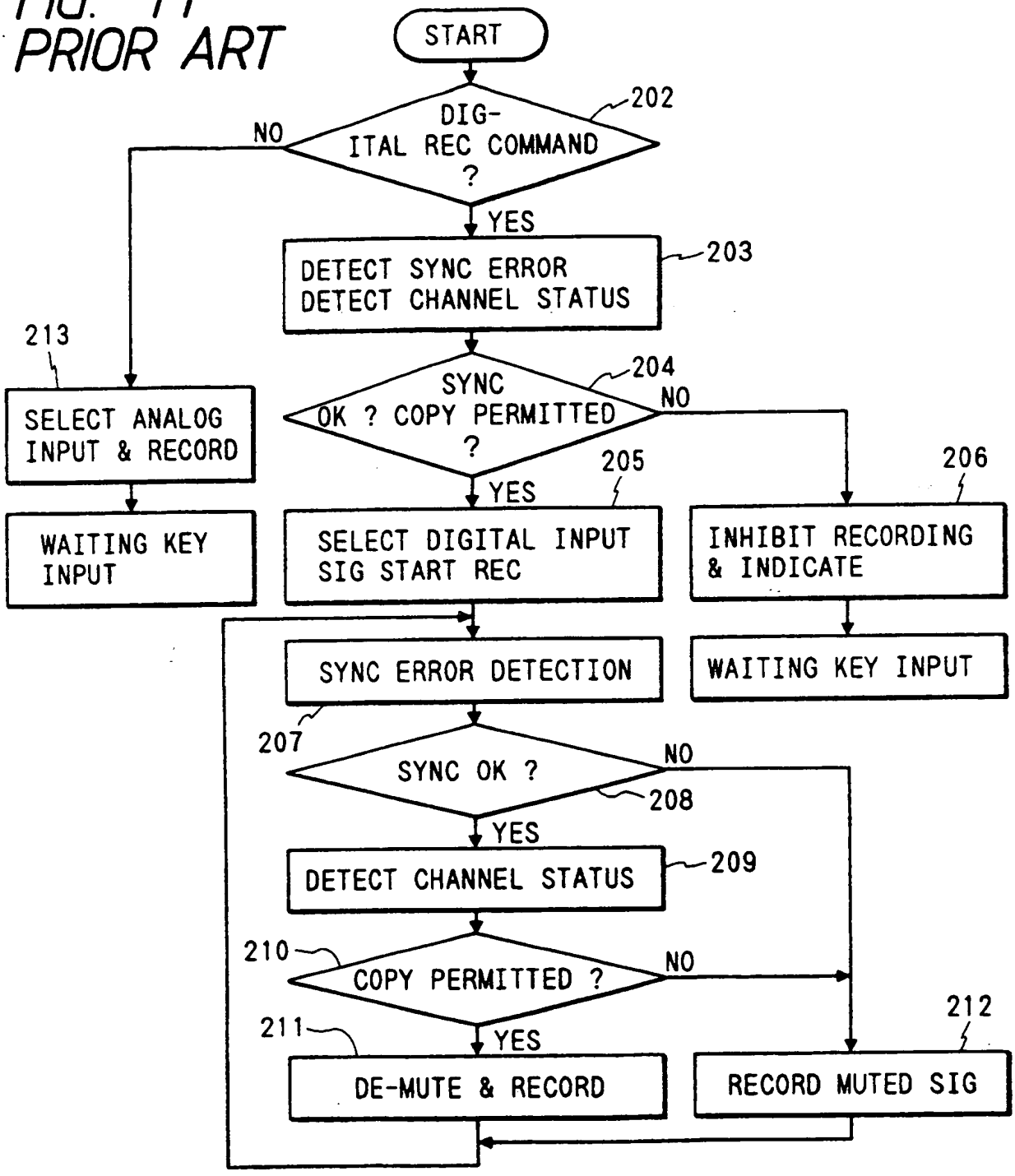


FIG. 10
PRIOR ART

FIG. 11
PRIOR ART



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European Patent Office
Office européen des brevets

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14.09.89 JP 238525/89

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(54) Data recording apparatus.

(57) A data recording apparatus comprises a digital input processing circuit, an analog input processing circuit including an A/D converter (11) for recording the analog input signal in a digital form, a switch (30) for selecting either digital or analog input signal for recording, and a control circuit (40). Normally, the apparatus records the digital input signal. When the digital input processing circuit detects a synchronizing error or inhibition of recording the digital input signal (digital copy) by analyzing the sub-code signal of the digital input signal, the control circuit (40) control the switch (30) so as to select the analog input signal. In order to reduce unnatural level variation due to change of selection between the digital and analog input signals, there are further provided a polarity change circuit (81), variable delay, and variable gain amplifier for the analog audio signal.

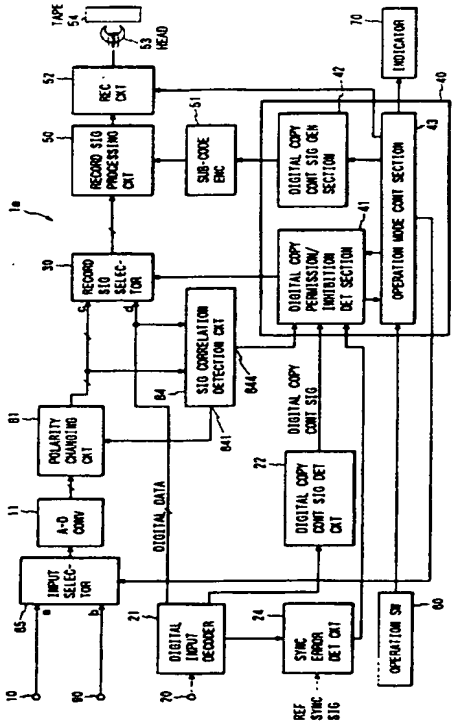

FIG. 1

EP 0 416 663 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 11 7393

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 13, no. 185 (P-865)(3533) 2 May 1989 & JP-A-1 013 260 (MITSUBISHI) 18 January 1989	3,4,6,9, 13,20	G 11 B 20/00 G 11 B 20/10
A	* abstract *	1	
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 185 (P-865)(3533) 2 May 1989 & JP-A-1 013 261 (AIWA CO LTD) 18 January 1989 * abstract * *	5-14	
A	EP-A-0 297 242 (KABUSHIKI KAISHA TOSHIBA) * column 10, line 6 - line 46 * * * column 16, line 19 - line 51; figures 6,7,15 * *	1,3,19,20	
A	EP-A-0 328 141 (MATSUSHITA) * column 3, line 12 - line 35 * * * column 4, line 6 - line 19; figures 2,3 * *	1,3	
A	WO-A-8 605 057 (WIJNEN) * page 1, line 1 - page 2, line 28 * *	1,2,19	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 11 B
H 04 N

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	19 December 91	BRUNET L.M.R.

CATEGORY OF CITED DOCUMENTS

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D : document cited in the application
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